IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A signal processing circuit in an image input apparatus which stores, in storage units of a main memory, a unit image signal in predetermined units that is obtained by an image pickup device and arranged in two dimensions, said signal processing circuit reading and processing said unit image signal stored in said main memory,

said signal processing circuit, comprising:

first and second storage ~~means~~ sections provided with a plurality of storage regions of the same number of bits as said unit image signal,

wherein said storage regions of said first storage ~~means~~ section and said storage regions of said second storage ~~means~~ section are connected to one another, such that an array of said unit image signal stored in said main memory is stored in said storage regions of said second storage ~~means~~ section in a state of being rotated 90 degrees clockwise~~, alternatively, 90 degrees counterclockwise, through proceeding that~~ when said unit image signal stored in said main memory is transferred and stored in said storage regions of said first storage ~~means~~ section, and then said unit image signal stored in said storage regions of said first storage ~~means~~ section is transferred and stored in said storage regions of said second storage ~~means~~ section.

Claim 2 (Currently Amended): A signal processing circuit of an image input apparatus, comprising:

first and second storage ~~means~~ sections provided with a plurality of storage regions of the same number of bits as a unit image signal in predetermined units that is obtained by an image pickup device in said image input apparatus and arranged in two dimensions,

wherein said storage regions of said first storage ~~means~~ section and said storage regions of said second storage ~~means~~ section are directly connected to one another by a predetermined connecting line, such that an array of said unit image signal stored in said storage regions of said first storage ~~means~~ section is reflected about a centerline of said array, to be stored in said storage regions of said second storage ~~means~~ section.

Claim 3 (Currently Amended): A signal processing circuit of an image input apparatus, comprising:

first and second register groups provided with a plurality of storage regions of the same number of bits as a unit image signal in predetermined units that is obtained by an image pickup device in said image input apparatus and arranged in two dimensions, said first and second register groups having first to fourth registers, respectively, said first to fourth registers having zero-th to third storage regions, respectively,

wherein said zero-th storage regions of said first to fourth registers of said first register group are connected directly, by a predetermined connecting line, to said zero-th to third storage regions of said fourth register of said second register group[[;]],

said first storage regions of said first to fourth registers of said first register group are connected directly, by a predetermined connecting line, to said zero-th to third storage regions of said third register of said second register group[[;]],

said second storage regions of said first to fourth registers of said first register group are connected directly, by a predetermined connecting line, to said zero-th to third storage regions of said second register of said second register group[[;]], and

said third storage regions of said first to fourth registers of said first register group are connected directly, by a predetermined connecting line, to said zero-th to third storage regions of said first register of said second register group.

Claim 4 (Currently Amended): A signal processing circuit of an image input apparatus, comprising:

first and second register groups provided with a plurality of storage regions of the same number of bits as a unit image signal in predetermined units that is obtained by an image pickup device in said image input apparatus and arranged in two dimensions, said first and second register groups having first to fourth registers, respectively, said first to fourth registers having zero-th to third storage regions, respectively,

wherein said zero-th storage regions of said first to fourth registers of said first register group are connected directly, by a predetermined connecting line, to said zero-th to third storage regions of said fourth register of said second register group,

said first storage regions of said first to fourth registers of said first register group are connected directly, by a predetermined connecting line, to said zero-th to third storage regions of said third register of said second register group,

said second storage regions of said first to fourth registers of said first register group are connected directly, by a predetermined connecting line, to said zero-th to third storage regions of said second register of said second register group, and

said third storage regions of said first to fourth registers of said first register group are connected directly, by a predetermined connecting line, to said zero-th to third storage regions of said first register of said second register group; and

~~The signal processing circuit of an image input apparatus according to claim 3, further comprising:~~

a third register group having first to fourth registers which are respectively provided with zero-th to third storage regions of the same number of bits as a unit image signal in predetermined units arranged in two dimensions,

wherein said zero-th to third storage regions of said first register of said second register group are connected directly, by a predetermined connecting line, to said third to zero-th storage regions of said first register of said third register group, respectively[[;]],

said zero-th to third storage regions of said second register of said second register group are connected directly, by a predetermined connecting line, to said third to zero-th storage regions of said second register of said third register group, respectively[[;]],

said zero-th to third storage regions of said third register of said second register group are connected directly, by a predetermined connecting line, to said third to zero-th storage regions of said third register of said third register group, respectively[[;]], and

said zero-th to third storage regions of said fourth register of said second register group are connected directly, by a predetermined connecting line, to said third to zero-th storage regions of said fourth register of said third register group, respectively.

Claim 5 (Original): A signal processing circuit of an image input apparatus, comprising:

second and third register groups provided with a plurality of storage regions of the same number of bits as a unit image signal in predetermined units that is obtained by an image pickup device in said image input apparatus and arranged in two dimensions, said second and third register groups having first to fourth registers, said first to fourth registers having zero-th to third storage regions,

wherein said zero-th to third storage regions of said first register of said second register group are connected directly, by a predetermined connecting line, to said third to zero-th storage regions of said first register of said third register group, respectively;

said zero-th to third storage regions of said second register of said second register group are connected directly, by a predetermined connecting line, to said third to

zero-th storage regions of said second register of said third register group, respectively;

said zero-th to third storage regions of said third register of said second register group are connected directly, by a predetermined connecting line, to said third to zero-th storage regions of said third register of said third register group, respectively; and

said zero-th to third storage regions of said fourth register of said second register group are connected directly, by a predetermined connecting line, to said third to zero-th storage regions of said fourth register of said third register group, respectively.

Claim 6 (Withdrawn): A signal processing circuit of an image input apparatus, comprising:

first and second storage means provided with a plurality of storage regions of the same number of bits as a unit image signal in predetermined units that is obtained by an image pickup device in said image input apparatus and arranged in two dimensions,

wherein said unit image signal is one of a plurality of components forming a predetermined unit of arrangement of color components; and

said storage regions of said first storage means and said storage regions of said second storage means are directly connected one another by a predetermined connecting line, such that an array of said unit image signal stored in said storage regions of said first storage means is stored in said storage regions of said second storage means, along with a rotation conversion in which an array of said unit image signal stored in said storage regions of said first storage means is rotated 90 degrees clockwise, alternatively, 90 degrees counterclockwise, while maintaining said unit of arrangement of color components.

Claim 7 (Withdrawn): The signal processing circuit of an image input apparatus according to claim 6, wherein

said rotation conversion is to perform only a clockwise 90 degrees rotation;

said unit of arrangement of color components is composed of one brightness component and two color components of which frequency in the horizontal or vertical allocation is one-half the frequency in the horizontal or vertical allocation of said brightness component; and

a first register group is provided as said first storage means, and a second register group is provided as said second storage means, each of said first and second register groups having first and second registers, each of said first and second registers having zero-th to third storage regions storing said brightness component and said two color components;

and wherein said zero-th storage region of said first register of said first register group is connected directly, by a predetermined connecting line, to said zero-th storage region of said second register of said second register group;

said second storage region of said first register of said first register group is connected directly, by a predetermined connecting line, to said zero-th storage region of said first register of said second register group;

said zero-th storage region of said second register of said first register group is connected directly, by a predetermined connecting line, to said second storage region of said second register of said second register group;

said first storage region of said second register of said first register group is connected directly, by a predetermined connecting line, to said first storage region of said first register of said second register group and to said first storage region of said second register of said second register group;

said second storage region of said second register of said first register group is connected directly, by a predetermined connecting line, to said second storage region of said first register of said second register group; and

said third storage region of said second register of said first register group is connected directly, by a predetermined connecting line, to said third storage region of said first register of said second register group and to said third storage region of said second register of said second register group.

Claim 8 (Withdrawn): The signal processing circuit of an image input apparatus according to claim 6, wherein

said rotation conversion is to perform only a counterclockwise 90 degrees rotation;

said unit of arrangement of color components is composed of one brightness component and two color components of which frequency in the horizontal or vertical allocation is one-half the frequency in the horizontal or vertical allocation of said brightness component; and

first register group is provided as said first storage means, and second register group is provided as said second storage means, each of said first and second register groups having the first and second registers, each of said first and second registers having zero-th to third storage regions storing said brightness component and said two color components;

and wherein said zero-th storage region of said first register of said first register group is connected directly, by a predetermined connecting line, to said second storage region of said first register of said second register group;

said second storage region of said first register of said first register group is connected directly, by a predetermined connecting line, to said second storage region of said second register of said second register group;

said zero-th storage region of said second register of said first register group is connected directly, by a predetermined connecting line, to said zero-th storage region of said first register of said second register group;

said first storage region of said second register of said first register group is connected directly, by a predetermined connecting line, to said first storage region of said first register of said second register group and to said first storage region of said second register of said second register group;

said second storage region of said second register of said first register group is connected directly, by a predetermined connecting line, to said zero-th storage region of said second register of said second register group; and

said third storage region of said second register of said first register group is connected directly, by a predetermined connecting line, to said third storage region of said first register of said second register group and to said third storage region of said second register of said second register group.

Claim 9 (Withdrawn): A signal processing circuit of an image input apparatus, comprising:

storage means provided with a plurality of storage regions of the same number of bits as a unit image signal in predetermined units that is obtained by an image pickup Device in said image input apparatus and arranged in two dimensions, said unit image signal being one of a plurality of components forming a predetermined unit of arrangement of color components; and

clockwise rotation means with which, in response to input of a predetermined clockwise rotation instruction signal, an array of a unit image signal that is stored in said

storage regions of said storage means is rotated 90 degrees clockwise, while maintaining said unit of arrangement of color components, and then stored in said storage regions of said storage means.

Claim 10 (Withdrawn): The signal processing circuit of an image input apparatus according to claim 9, wherein

said unit of arrangement of color components is composed of one brightness component and two color components of which frequency in the horizontal or vertical allocation is one-half the frequency in the horizontal or vertical allocation of said brightness component; and

a register group is provided as said storage means, said register group having first and second registers, each of said first and second registers having zero-th to third storage regions storing said brightness component and said two color components;

and wherein in response to input of said clockwise rotation instruction signal, with said clockwise rotation means,

a unit image signal in said zero-th storage region of said first register is stored in said zero-th storage region of said second register;

a unit image signal in said second storage region of said first register is stored in said zero-th storage region of said first register;

a unit image signal in said zero-th storage region of said second register is stored in said second storage region of said second register;

a unit image signal in said first storage region of said second register is stored in said first storage region of said first register and said first storage region of said second register;

a unit image signal in said second storage region of said second register is stored in said second storage region of said first register; and

a unit image signal in said third storage region of said second register is stored in said third storage region of said first register and said third storage region of said second register.

Claim 11 (Withdrawn): A signal processing circuit of an image input apparatus, comprising:

storage means provided with a plurality of storage regions of the same number of bits as a unit image signal in predetermined units that is obtained by an image pickup device in said image input apparatus and arranged in two dimensions,

wherein said unit image signal is one of a plurality of components forming a predetermined unit of arrangement of color components; and

counterclockwise rotation means with which, in response to input of a predetermined counterclockwise rotation instruction signal, an array of a unit image signal that is stored in said storage regions of said storage means is rotated 90 degrees counterclockwise, while maintaining said unit of arrangement of color components, and then stored in said storage regions of said storage means.

Claim 12 (Withdrawn): The signal processing circuit of an image input apparatus according to claim 11, wherein

said unit of arrangement of color components is composed of one brightness component and two color components of which frequency in the horizontal or vertical allocation is one-half the frequency in the horizontal or vertical allocation of said brightness component; and

a register group is provided as said storage means, said register group having first and second registers, each of said first and second registers having zero-th to third storage regions storing said brightness component and said two color components;

and wherein in response to input of said counterclockwise rotation instruction signal, with said counterclockwise rotation means;

a unit image signal in said zero-th storage region of said first register is stored in said second storage region of said first register;

a unit image signal in said second storage region of said first register is stored in said second storage region of said second register;

a unit image signal in said zero-th storage region of said second register is stored in said zero-th storage region of said first register;

a unit image signal in said first storage region of said second register is stored in said first storage region of said first register and said first storage region of said second register;

a unit image signal in said second storage region of said second register is stored in said zero-th storage region of said second register; and

a unit image signal in said third storage region of said second register is stored in said third storage region of said first register and said third storage region of said second register.

Claim 13 (Withdrawn): A signal processing circuit of an image input apparatus, comprising:

first and second storage means provided with a plurality of storage regions of the same number of bits as a unit image signal in predetermined units that is obtained by an image pickup device in said image input apparatus and arranged in two dimensions,

wherein said unit image signal is one of a plurality of components forming a predetermined unit of arrangement of color components; and

said storage regions of said first storage means and said storage regions of said second storage means are directly connected one another by a predetermined connecting line, such that each of unit image signals stored in said storage regions in order to form a first unit

of arrangement of color components in said first storage means, is converted to a second unit of arrangement of color components, and then stored in said storage regions of said second storage means.

Claim 14 (Withdrawn): The signal processing circuit of an image input apparatus according to claim 13, wherein

said first and second unit of arrangement of color components are composed of one brightness component and two color components of which frequency in the horizontal or vertical allocation is one-half the frequency in the horizontal or vertical allocation of said brightness component; and

a first register is provided as said first storage means, and a second register is provided as said second storage means, each of said first and second registers having the zero-th to third storage regions storing said brightness component and said two color components;

and wherein said zero-th storage region of said first register is connected directly to said zero-th storage region of said second register by a predetermined connecting line;

said first storage region of said first register is connected directly to said second storage region of said second register by a predetermined connecting line;

said second storage region of said first register is connected directly to said first storage region of said second register by a predetermined connecting line; and

said third storage region of said first register is connected directly to said third storage region of said second register by a predetermined connecting line.

Claim 15 (New): The signal processing circuit of Claim 1, wherein an array of said unit image signal stored in said main memory is stored in said storage regions of said second

storage section in a state of being rotated 90 degrees counterclockwise when said unit image signal stored in said main memory is transferred and stored in said storage regions of said first storage section, and then said unit image signal stored in said storage regions of said first storage section is transferred and stored in said storage regions of said second storage section.